(19) Europäisches Patentamt
European Pat nt Office
Office européen d s brev ts

(11) Publication number : **0 609 882 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **94101651.1**

(22) Date of filing : **03.02.94**

(51) Int. Cl.^{5} : **G11B 7/09**

(30) Priority : **05.02.93 JP 42137/93**

(43) Date of publication of application : **10.08.94 Bulletin 94/32**

(84) Designated Contracting States : **DE FR GB**

(71) Applicant : **SONY CORPORATION**
7-35, Kitashinagawa 6-chome
Shinagawa-ku
Tokyo (JP)

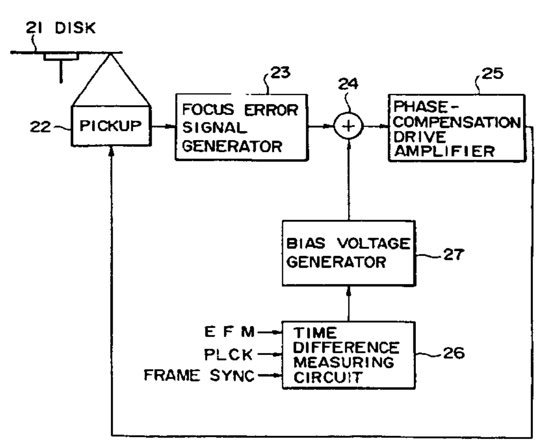
(72) Inventor : **Shimizume, Kazutoshi, c/o Sony Corporation**
7-35, Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)
Inventor : **Akita, Mamoru, c/o Sony Corporation**
7-35, Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)
Inventor : **Inohana, Shigeru, c/o Sony Corporation**
7-35, Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)
Inventor : **Noda, Hidenobu, c/o Sony Corporation**
7-35, Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)

(74) Representative : **Melzer, Wolfgang, Dipl.-Ing. et al**
Patentanwälte,
Mitscherlich & Partner,
Sonnenstrasse 33
D-80331 München (DE)

(54) Automatic bias adjustment for focus servo circuit.

(57) In a recording and reproducing apparatus of CD (21) or the like, it is adapted such that the quantity ofjitters in an RF signal is measured as a time difference between an edge of a PLL clock synchronized with an EFM signal and a transition point of the EFM signal in a time difference measuring circuit, a focus bias voltage to bring the time difference to a minimum is established in a bias voltage generator (27), the established focus bias voltage is added in an adder to a focus error signal generated in a focus error signal generator (23), and, thereby, the focus bias is automatically adjusted and focus servo is executed in accordance with the bias-adjusted focus error signal.

F I G. 3



EP 0 609 882 A1

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a focus servo circuit and, more particularly, to a focus servo circuit suitable for use in the servo system of optical disk players such as CD (Compact Disk) players.

2. Description of the Related Art

A focus servo circuit is indispensable to optical disk players, for example CD players, which focus servo circuit executes control while the disk is rotated to keep the distance between the objective lens incorporated in the pickup and the signal surface of the disk constant against vertical movements of the signal surface of the disk due to a warp or the like of the disk.

An example of a focus servo circuit of the related art is shown in FIG. 1, in which a pickup 2 optically reading signal information on a disk 1 supplies an output of a focus servo system to a focus error signal generator 3.

In the focus error signal generator 3, a focus error signal, which becomes zero when the signal surface of the disk lies on the focal plane of the optic system, becomes minus (or plus) when the signal surface comes closer to the objective lens, and becomes plus (or minus) when the signal surface goes away from the objective lens, is generated according to a known method such as the astigmatic method.

The focus error signal, after being passed through an adder 4, is compensated for phase in a phase-compensation drive amplifier 5 and supplied to a focus actuator, within the pickup 2, as its drive signal.

When for example the astigmatic method is used as the method of generating the focus error signal in the focus error signal generator 3, a quadrant sensor 11 having its photosensing surface divided into four parts is used as the photosensor in the pickup 2 as shown in FIG. 2. Outputs of the photosensing parts (1) and (3), and (2) and (4), both diagonally disposed, are added in adders 12 and 13, respectively, and the added outputs are then subjected to subtraction in a subtractor 14, and thereby a focus error signal is generated. Because of such structure, if there are variations in sensitivity among the photosensing parts (1) to (4) of the quadrant sensor 11, or if there are some offsets in the circuit systems such as the adders, it sometimes occurs that a component related to the offset is produc d in the focus error signal, and hence, even wh n th signal surface of the disk is on the focal plan , th focus rror signal does not become zero.

If the focus servo is carri d out under the described state, a defocus corresponding to th component related to the offset is produced and therefore it becomes imp ssible to read well the signal information on the disk.

Therefore, it has so far been practiced to generate a bias voltage using a semi-fixed resistor R and add this bias voltage to the focus error signal in th adder 4 to thereby cancel the component related to the offset and achieve offset adjustments of focus servo to bring about a just-in-focus state.

The bias adjustment of the focus servo has been carried out in the production line such that the position of the pit on the disk comes into focus, i.e., such that the eye pattern of an RF signal output from th pickup 2 becomes cleanest in the waveform observation.

In the focus servo circuit of the related art of th described structure, however, the bias adjustment of the focus servo in the production line has been mad manually. Therefore, there have been such problems that the adjustment requires skill and time and, in addition, such defocuses that occur in the cases where the thickness or material of the actually reproduced disk is varied causing variations in refractive index cannot be coped with.

OBJECT AND SUMMARY OF THE INVENTION

The present invention has been made in view of the above mentioned problems. Accordingly, it is an object of the present invention to provide a focus servo circuit capable of making bias adjustment of the focus servo automatically and most suitably for each reproduced disk.

A focus servo circuit according to the invention comprises a focus error signal generator for generating a focus error signal, a time difference measuring circuit for measuring a time difference between an edge of a clock synchronized with a binarized signal reproduced from a disk and a transition point of the binarized signal, a bias voltage generator for generating a focus bias voltage corresponding to the time difference, and an adder for adding the focus bias voltage to the focus error signal, and in which it is adapted such that focus servo is carried out in accordance with the added output in the adder.

With the described arrangement, a quantity of jitters in an RF signal is measured as the time difference between an edge of a clock synchronized with a binarized signal and a transition point of the binarized signal. Since the quantity of jitters is correspondent to the focus bias error, the focus bias voltage is established so that the time difference may be minimized.

The stablish d focus bias voltage is added to the focus error signal. Thereby, a DC offs t component contain d in the focus error signal is canceled, and thus, automatic adjustments to bring a focus biased state into a just-in-focus state can b ach-

ieved.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a focus servo circuit of a related art;
FIG. 2 is a block diagram explanatory of the principle of an astigmatic method of a related art;
FIG. 3 is a block diagram showing a first embodiment of a focus servo circuit according to the invention;
FIGs. 4A and 4B are waveform diagrams of an RF signal and a PLL clock in the servo circuit shown in FIG. 3, of which FIG. 4A shows them in a just-in-focus state and FIG. 4B shows them in an out-of-focus state;
FIGs. 5A and 5B are waveform diagrams of an EFM signal and the PLL clock, of which FIG. 5A shows them in a just-in-focus state and FIG. 5B shows them in an out-of-focus state;
FIG. 6 is a diagram showing a time difference $\pm\Delta\theta$ between the EFM signal and the PLL clock;
FIG. 7 is a block diagram showing an example of structure of a time difference measuring circuit as a second embodiment of the invention;
FIG. 8 is a diagram showing waveforms in various parts of the time difference measuring circuit shown in FIG. 7;
FIG. 9 is a characteristic diagram showing results of measurement of block error rates and number of times of phase deviations with respect to focus bias voltages;
FIG. 10 is a characteristic diagram of focus bias voltage versus number of times of phase deviations based on results of measurement; and
FIG. 11 is a flow chart showing an example of steps followed in establishing a bias voltage.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will be described below in detail with reference to the accompanying drawings.

FIG. 3 is a block diagram showing a first embodiment of a focus servo circuit according to the invention applied to a CD player.

Referring to FIG. 3, there is recorded signal information as a pit string on the signal surface of a disk 21. The signal information on the disk 21 is optically read by a pickup 22.

An RF signal output from the pickup 22 is supplied to a PLL circuit, not shown, and used for generation of a PLL clock PLCK synchronized with the RF signal and also suppli d to a digital signal processing syst m, not shown, and subj cted to signal processing th rein such as EFM (Eight to Fourteen Modulation) demodulation and rror correction, with the PLL clock PLCK used as a reference, and output therefrom as an audio signal.

A focus rror signal g n rator 23, according to a known generating method such as the astigmatic method, generates a focus error signal, which b - comes zero when the signal surface of the disk lies on the focal plane of the optic system, becomes minus (or plus) when the signal surface comes clos r to the objective lens, and becomes plus (or minus) when the signal surface goes away from the objective lens.

The focus error signal, after being pass d through an adder 24, is compensated for phase in a phase-compensation drive amplifier 25 and supplied to the focus actuator, within the pickup 22, as its driv signal.

In the execution of focus servo, referring to FIG. 4, when the system is in a just-in-focus state (FIG. 4A), the RF signal takes on a clean waveform and th PLL clock PLCK also takes on a waveform free of jitters, but if the system is somewhat deviated from the just-in-focus point, i.e., if it is out of focus (FIG. 4B), the frequency spectrum of the RF signal becomes broadened electrically and the RF signal takes on a dirty waveform and, hence, the PLL clock PLCK also takes on a waveform containing jitters.

FIG. 5A and FIG. 5B show waveforms of the EFM signal as a binarized signal of the RF signal and the PLL clock PLCK correspondently to FIG. 4A and FIG. 4B, respectively.

Accordingly, in the present invention, taking notice of the fact that the quantity of the jitters in the RF signal is minimized in the just-in-focus state, it is arranged such that the quantity of jitters corresponding to the focus bias error is measured as the time difference (phase difference) $\pm\Delta\theta$ between the edge of the PLL clock PLCK and the transition point of the EFM signal and the focus bias voltage is established to minimize the time difference $\pm\Delta\theta$ and, thereby, the bias adjustments are automatically achieved.

More specifically, referring to FIG. 3, there are provided a time difference measuring circuit 26 for measuring the time difference $\pm\Delta\theta$ between the edge of the PLL clock PLCK and the transition point of the EFM signal and a bias voltage generator 27 for generating a focus bias voltage corresponding to the time difference $\pm\Delta\theta$, and it is arranged such that the focus bias voltage is added in the adder 24 to the focus error signal to cancel the DC offset component generated in the servo system and, thereby, the bias adjustments are achieved.

The time difference measuring circuit 26 takes a predetermined length of time as a reference and counts th numb r of jitters, of which duration is ov r the r fer nce time (±Tref), occurring in one period (= 136 μs c.) of the frame sync signal, and measures the count value as the time diff r nce $\pm\Delta\theta$.

As the above reference tim (±Tr f), th tim N

times as large as the period corresponding to the frequency obtained by multiplying the frequency of the PLL clock PLCK (= 4.3218MHz) by 8 is established. When, for example, N = 3 is set, the time given below is taken as the reference:

$$Tref = (1/(4.3218MHz \times 8)) \times 3 \approx 88nsec. \quad (1)$$

The value of N is not limited to 3 but can be set to any desired value.

Below will be described a particular structure of a time difference measuring circuit 26 as a second embodiment of the invention.

FIG. 7 is a block diagram showing an example of the time difference measuring circuit 26. FIG. 8(a) to FIG. 8(e) show waveforms in the parts (a) to (e) in FIG. 7.

An EFM signal (b) becomes the input to a flip-flop 31 and also becomes one input to an exclusive OR gate 32. The flip-flop 31 is operated by a clock XPCK (a) obtained by inverting the PLL clock PLCK by an inverter 33. The output of the flip-flop 31 becomes the other input to the EX-OR gate 32.

Consequently, the output (c) of the EX-OR gate 32 takes on a high level during the period from the transition point of the EFM signal to the rising edge of the clock XPCK, i.e., the falling edge of the PLL clock PLCK.

The output (c) of the EX-OR gate 32 becomes a ci input to the 3-bit counter 34 and also becomes the input to a flip-flop 35.

The 3-bit counter 34, in which the value of (100) in the twos-complement expression (-4) is loaded as the initial value, counts, while the output (c) of the EX-OR gate 32 is at the high level, the clocks at the frequency 34MHz (≈ 4.3218MHz x 8). The count value (e) of the counter 34 corresponds to the time difference $\pm\Delta\theta$ between the transition point of the EFM signal and the edge of the PLL clock PLCK.

The output of the flip-flop 35 becomes the input to the flip-flop 36 and also becomes one input to a NAND gate 38 after being inverted by an inverter 37. Both the flip-flops 35 and 36 are operated by the clock 34mhz. The output of the flip-flop 36 becomes the other input to the NAND gate 38.

The output (d) of the NAND gate 38 becomes the load (LD) input to each of the 3-bit counter 34 and a register 39. In response to this load input (d), the final count of the 3-bit counter 34 is loaded into the register 39 and, at the same time, the aforesaid initial value (100) is loaded into the 3-bit counter 34.

The value (f) loaded into the register 39 becomes a compared input in a comparator 40. The comparator 40 generates an output at a high level when the value of the compared input is equal to or greater than for example ±3. By the numerical value "3", the reference time (±Tref) 88 nsec. given by the above expression (1) is established.

The output of the comparator 40 becomes one input to an AND gate 41. Th AND gate 41 receives th inverted output of the output (d) of the NAND gate 38 by an inverter 42 as the oth r input th reto and supplies th output of the comparator 40 to a counter 43 at the timing of generation of the output (d) of th NAND gate 38.

On the other hand, the output of the inverter 42 becomes one input to an AND gate 44 and the fram sync signal with a period of 136 μsec. becomes th other input to the same. The output of the AND gate 44 becomes the reset input to a counter 43 and further becomes the load input to a P/S (parallel/serial) register 45.

The P/S register 45 converts parallel data loaded from the counter 43 into serial data and, in respons to a shift in clock supplied from the bias voltage generator 27, outputs the serial data as shift out data to the bias voltage generator 27.

Here, the number of counts (number of times of phase deviations) obtained by counting measured changes of the RF signal deviating ±88 nsec. or more from the PLL clock PLCK during a period of 98 frames and the CI block error rates are shown in FIG. 9 as the results of measurement with the focus bias voltage taken as the parameter. In the diagram, the solid lines (a) indicate the block error rates and the broken lines (b) indicate the number of times of maximum phase deviations. Frequently observed values are within the regions surrounded by the two solid lines (a) and two broken lines (b).

As apparent from the results of the measurement, the focus bias voltage within the range from 0 to 0.3 V provides good results, and in this region both the CI block rate and the number of times of phase deviations are minimized.

A particular example in which a focus bias voltage is established in the bias voltage generator 27 in accordance with the data N (the number of times of phase deviations) measured in the time difference measuring circuit 26 will be described below.

The bias voltage generator 27, constituted of a microcomputer, establishes a focus bias voltage so that the average value of the measured data N may become a minimum.

An example of steps for establishing the bias voltage will be described below according to a flowchart of FIG. 11 based on the characteristic shown in FIG. 10.

First, the minimum value Nmin of the measured data N is measured (step S1), and then a threshold value Nth greater than the minimum value Nmin by α% is established (step S2). In establishing the threshold value Nth, it must be set below a limit value N_{LIM} at which it is possible that the focus servo loses its controlling function.

Th n, two bias valu s F_A and F_B with which the measured data N bec m s the thr shold value Nth are measured (step S3) and the average value of the two bias valu s F_A and F_B is obtained (step S4). This

average value is set to be the established focus bias voltage.

As described in the for going, according to the present invention, the quantity of jitters in an RF signal is measured as a time difference between an edge of a PLL clock synchronized with an EFM signal as a binarized signal and a transition point of the EFM signal and, then, a focus bias voltage bringing the time difference to a minimum is established. The established bias voltage is added to a focus error signal to thereby cancel an offset component. Thus, the bias adjustments, which have conventionally been performed in the product line, are made automatically attainable.

Further, by the attainment of automatic bias adjustments, the bias adjustments of the focus servo can be made every time a disk is reproduced. Accordingly, the reproduction can be achieved at a bias point most suitable for each disk in spite of variations of the disk in thickness or material.

Claims

1. A focus servo circuit comprising:

   a focus error signal generator (23) for generating a focus error signal;

   a time difference measuring circuit (26) for measuring a time difference between an edge of a clock synchronized with a binarized signal reproduced from a disk (21) and a transition point of said binarized signal;

   a bias voltage generator (27) for generating a focus bias voltage corresponding to said time difference; and

   an adder (24) for adding said focus bias voltage to said focus error signal, wherein

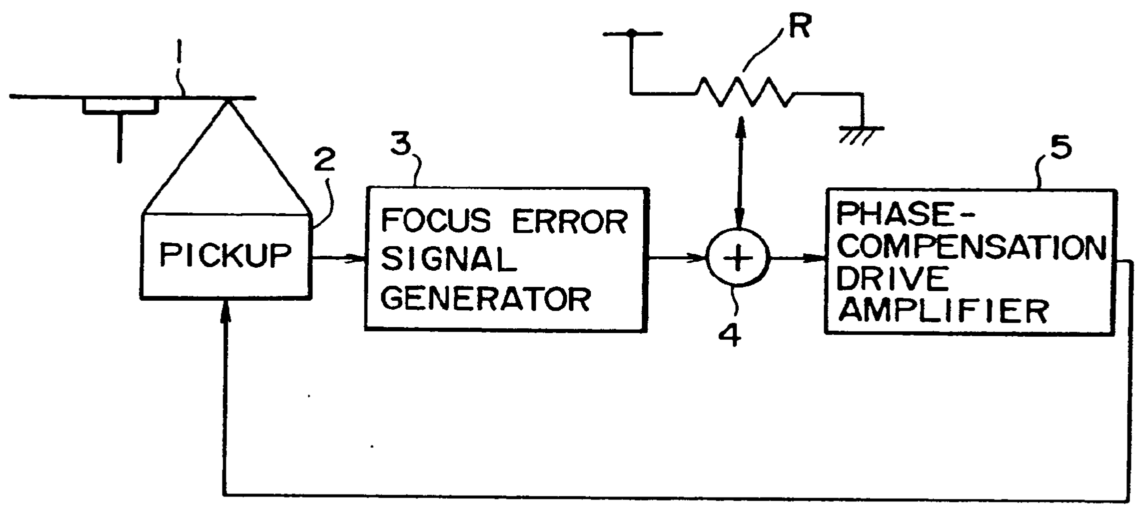
   focus servo is carried out in accordance with the added output in said adder.

2. A focus servo circuit according to claim 1, wherein said time difference measuring circuit (26) includes a circuit for measuring a time difference between an edge of said clock and a transition point of said binarized signal, a circuit for detecting an event of the measured time difference becoming equal to or greater than a reference time, and a counter for counting the number of said events detected within a predetermined interval of time, wherein count data of said counter is output as measured data of said time difference.

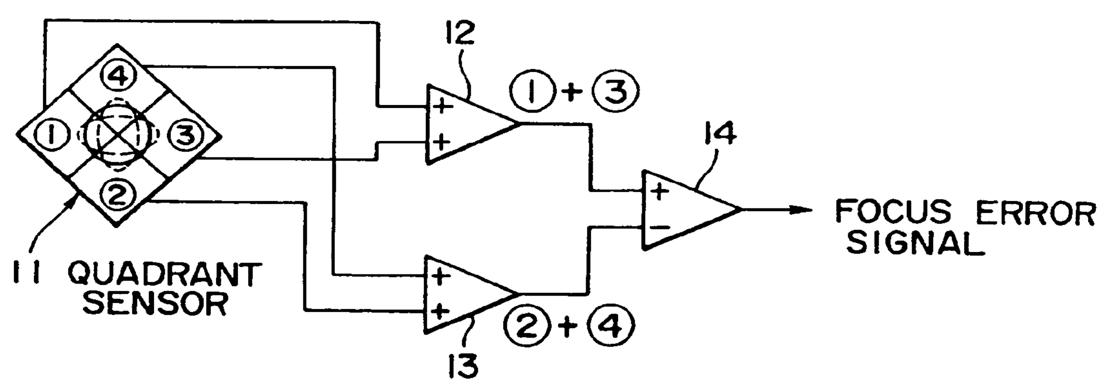
3. A focus servo circuit according to claim 2, wherein said bias voltag g n rator (27) stablishes said focus bias voltag so that th av rag valu of said measured data may becom a minimum.

4. A focus servo circuit according to claim 2, wherein said bias voltage generator (27) measures a minimum valu of said measured data, stablishes a threshold value greater than said minimum value by a predetermined value, measures two bias values with which said measured data becomes said threshold value, and establishes the average value of said two bias values as said focus bias voltage.

F I G. 1
RELATED ART



F I G. 2
RELATED ART



F I G. 3

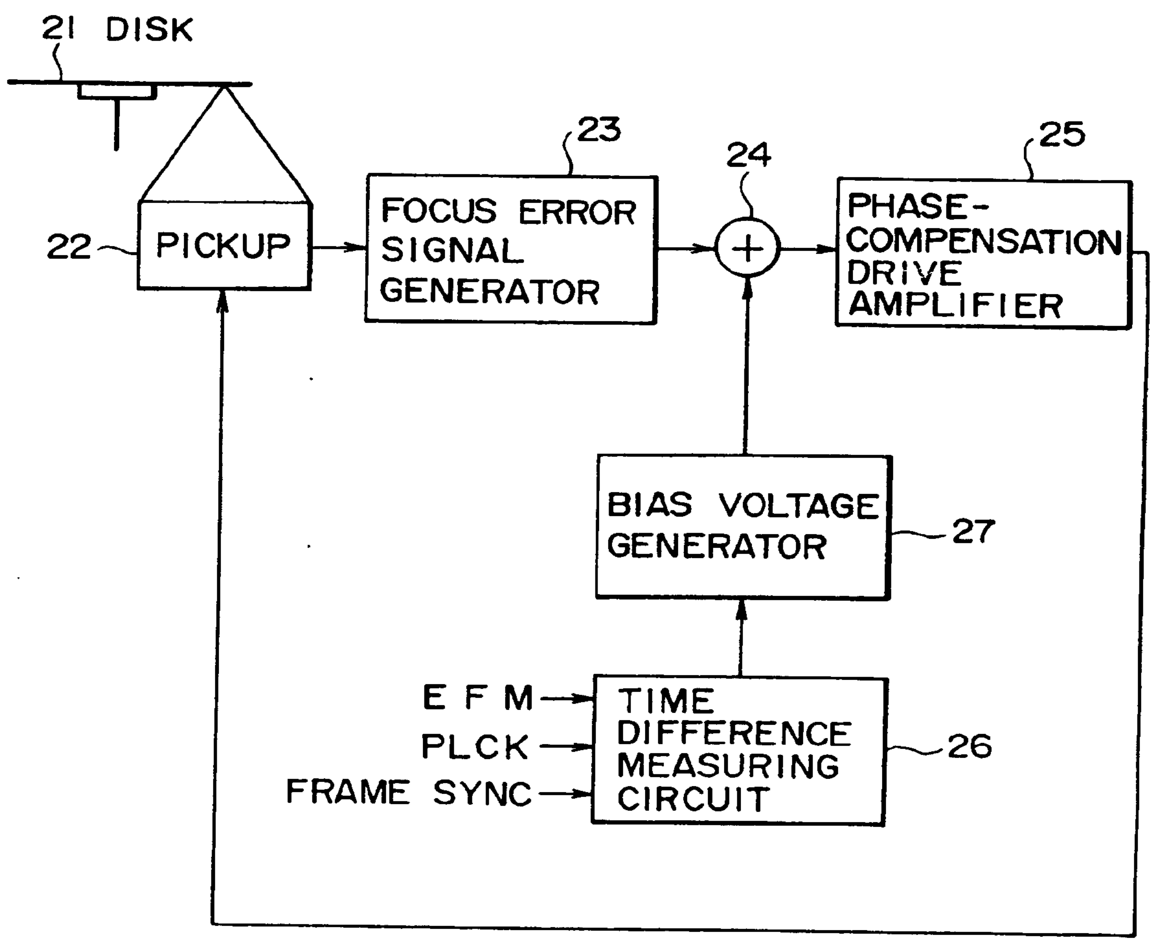

21 DISK
22
PICKUP
23
FOCUS ERROR SIGNAL GENERATOR
24
+
25
PHASE-COMPENSATION DRIVE AMPLIFIER
BIAS VOLTAGE GENERATOR
27
E F M
PLCK
FRAME SYNC
TIME DIFFERENCE MEASURING CIRCUIT
26

FIG. 4A RF SIGNAL AND PLL CLOCK IN JUST-IN-FOCUS STATE

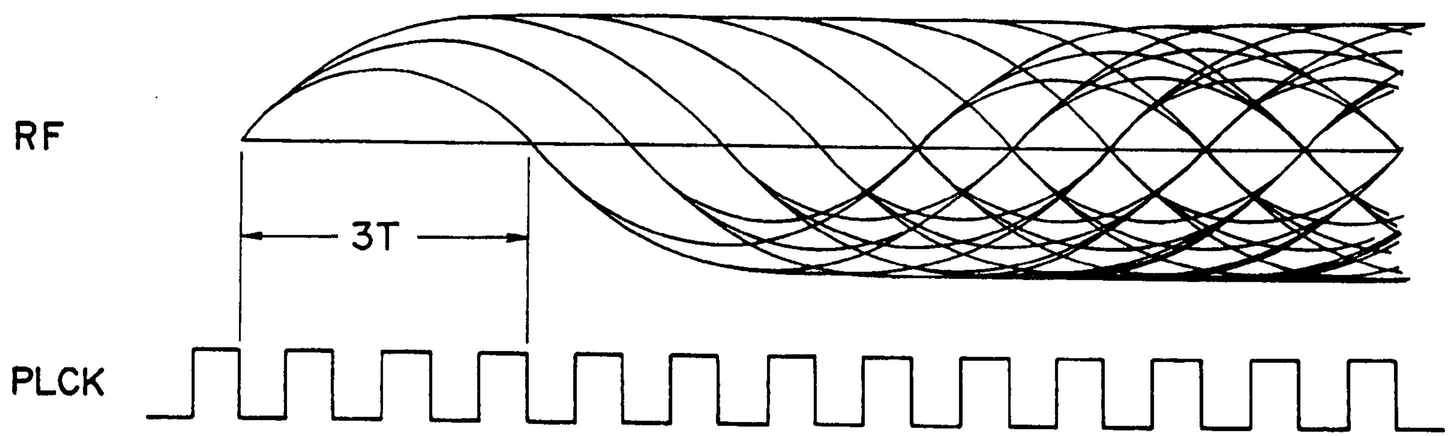


FIG. 4B RF SIGNAL AND PLL CLOCK IN OUT-OF-FOCUS STATE

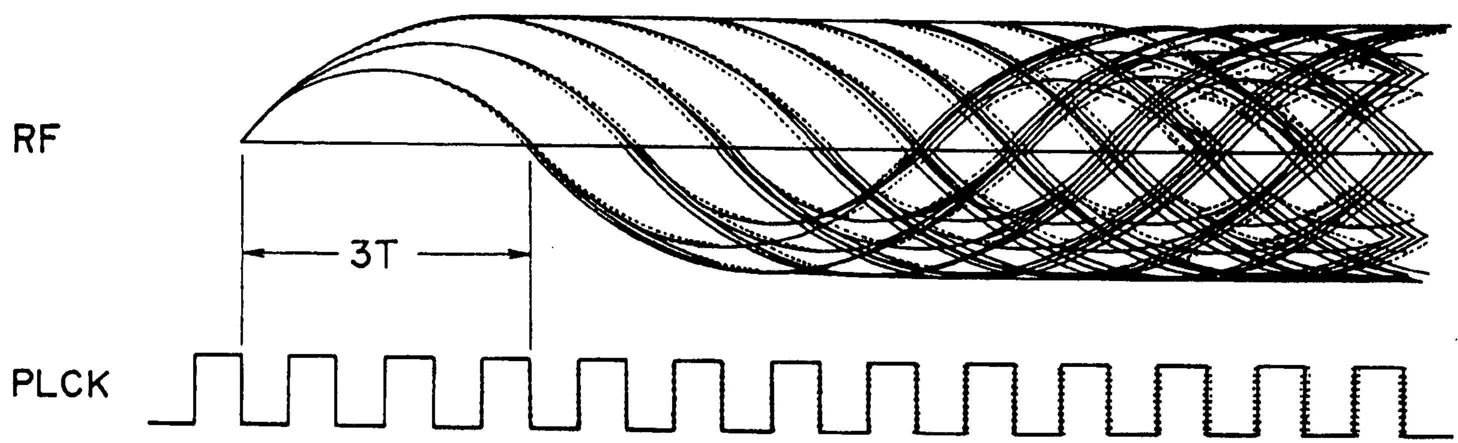


FIG. 5A EFM SIGNAL AND PLL CLOCK IN JUST-IN-FOCUS STATE

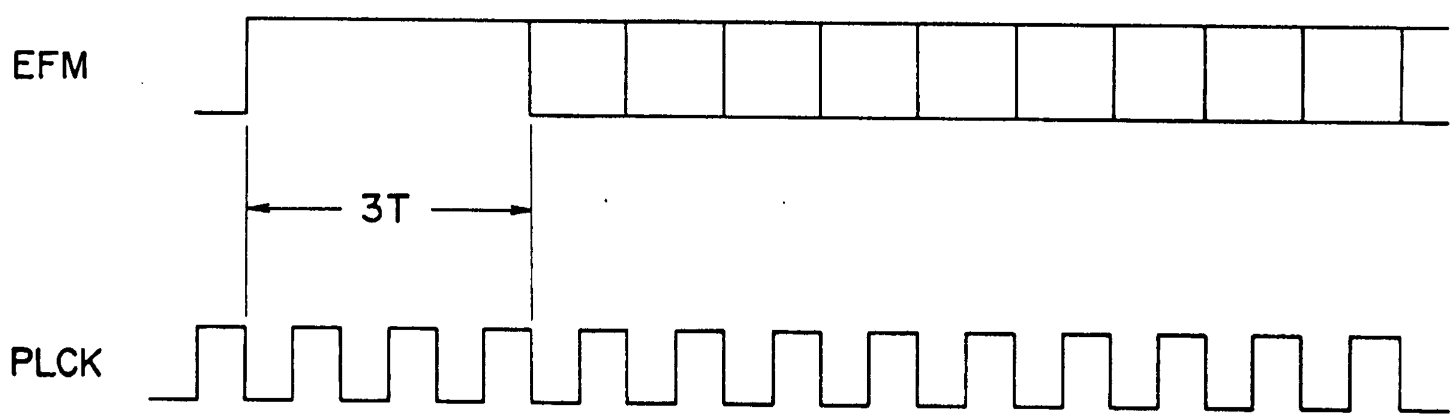


FIG. 5B EFM SIGNAL AND PLL CLOCK IN OUT-OF-FOCUS STATE

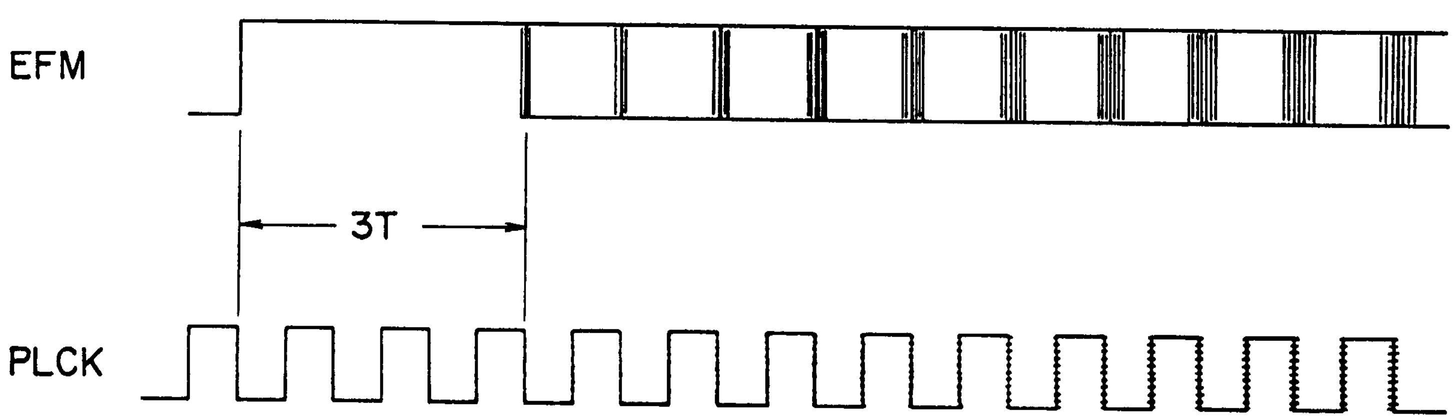
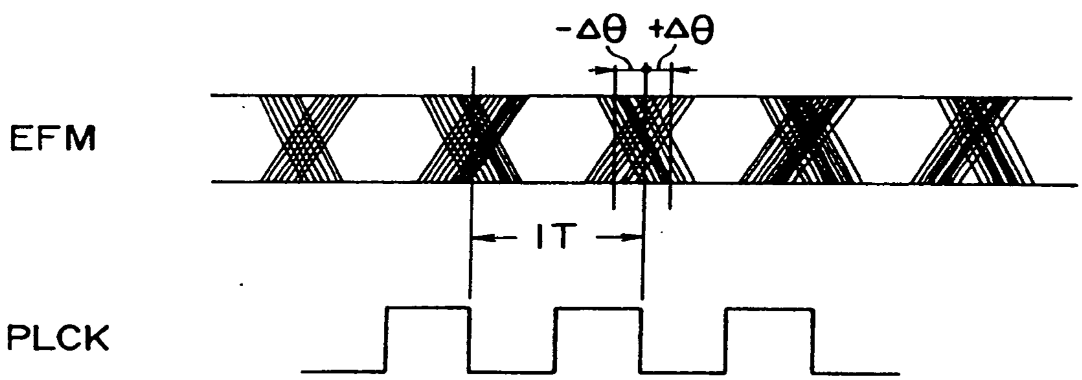
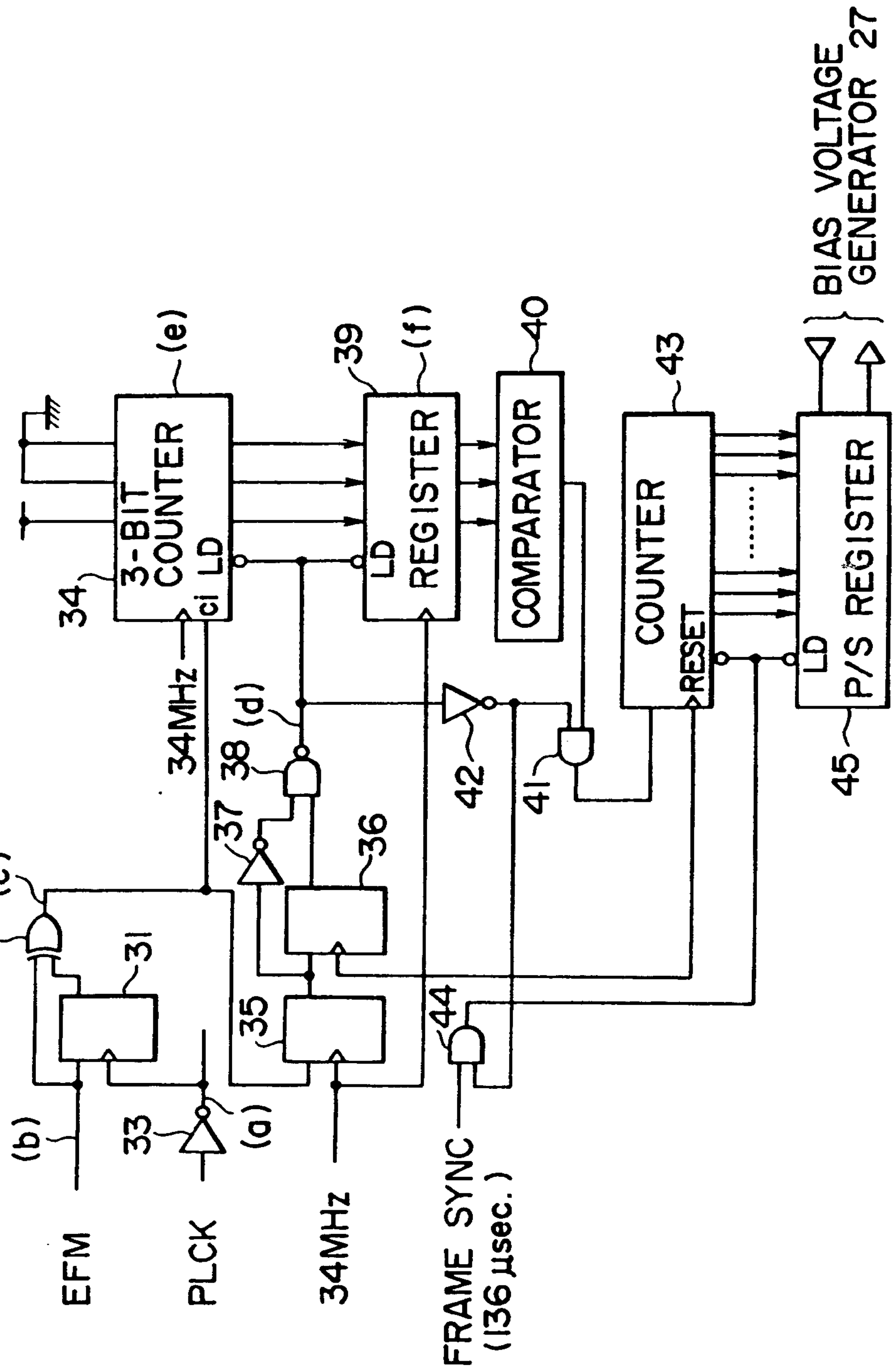


FIG. 6



F I G. 7


EFM
PLCK
34MHz
FRAME SYNC (136 µsec.)
(b)
(a)
(c)
(d)
(e)
(f)
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
3-BIT COUNTER
ci LD
34MHz
LD REGISTER
COMPARATOR
COUNTER
RESET
LD P/S REGISTER
BIAS VOLTAGE GENERATOR 27

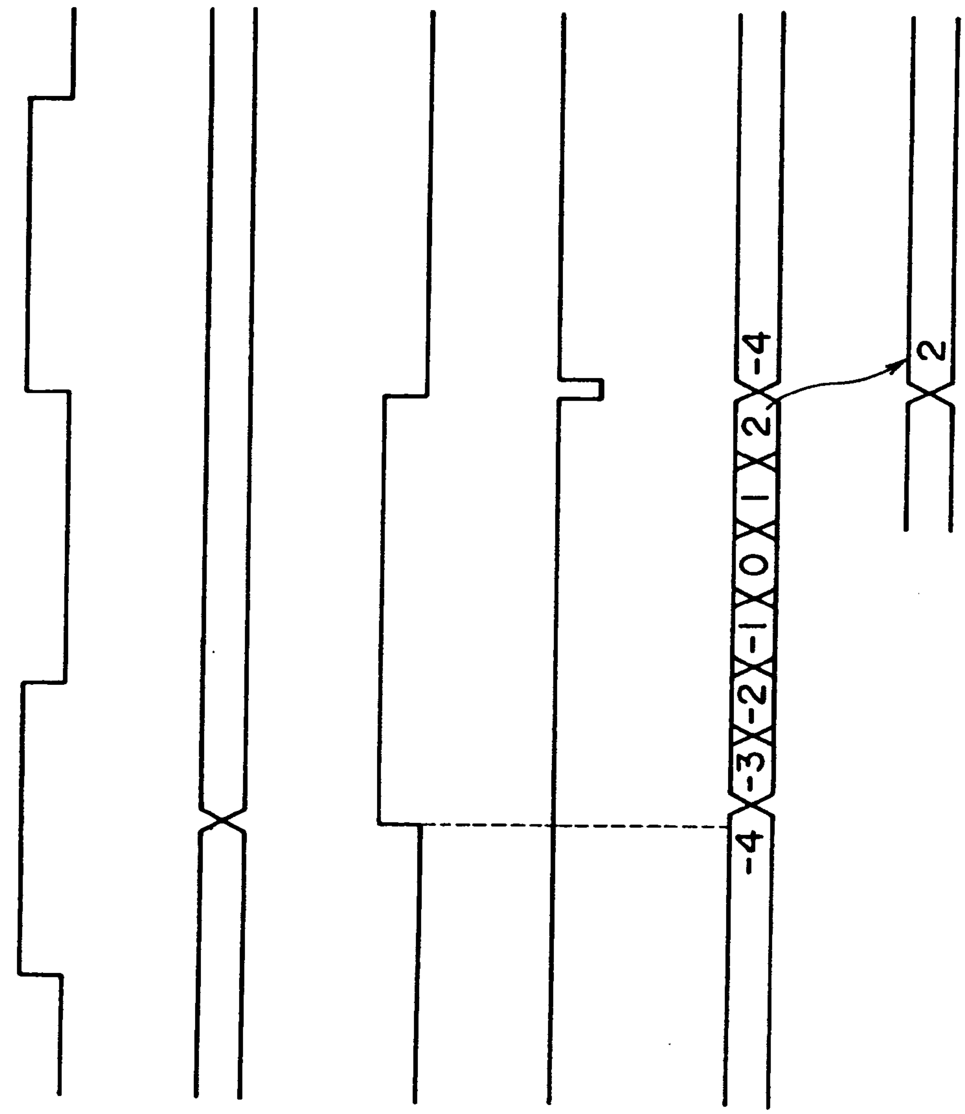


FIG. 8a

FIG. 8b

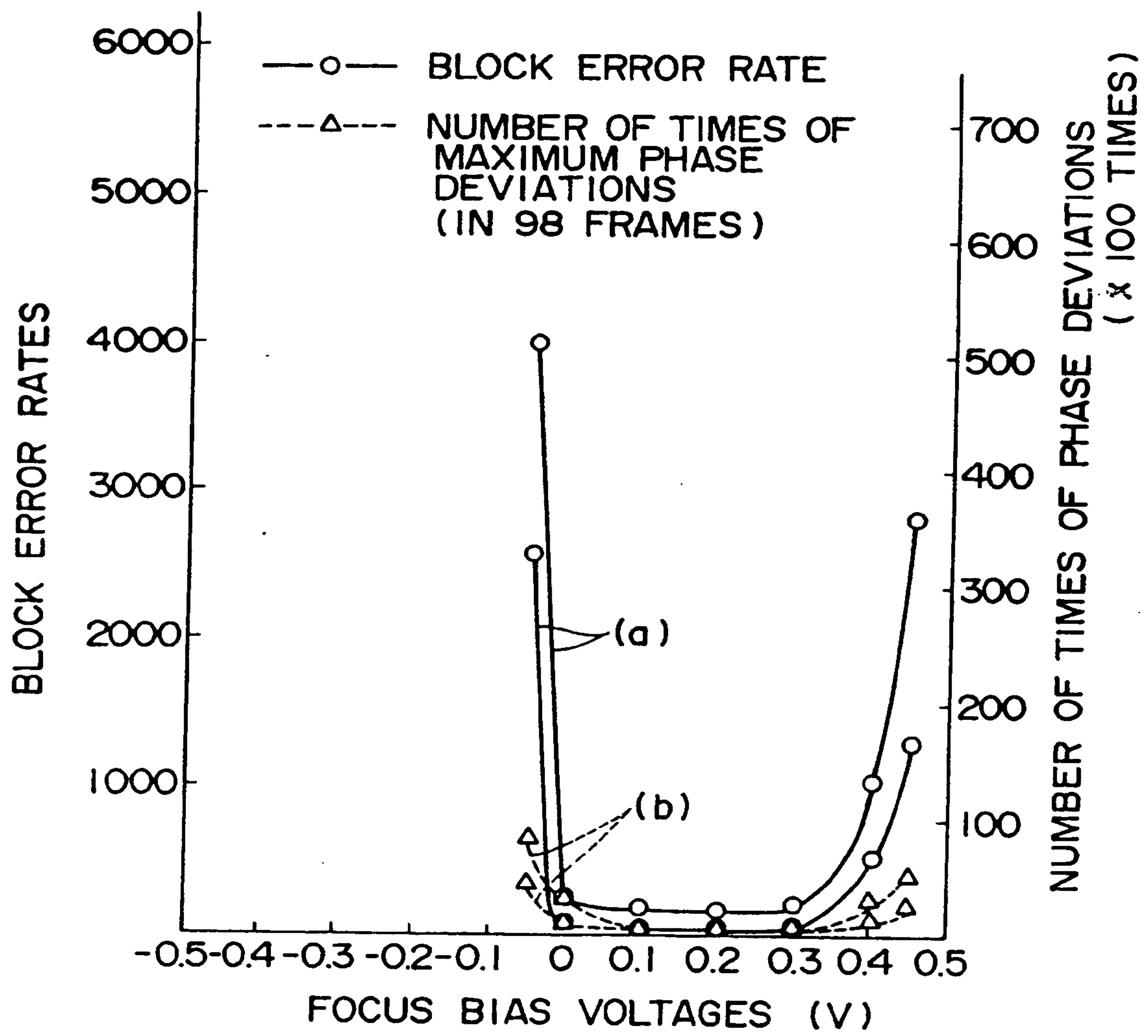
FIG. 8c

FIG. 8d

FIG. 8e

FIG. 8f

FIG. 9



BLOCK ERROR RATE
NUMBER OF TIMES OF MAXIMUM PHASE DEVIATIONS (IN 98 FRAMES)
BLOCK ERROR RATES
NUMBER OF TIMES OF PHASE DEVIATIONS (x 100 TIMES)
6000
5000
4000
3000
2000
1000
700
600
500
400
300
200
100
(a)
(b)
-0.5 -0.4 -0.3 -0.2 -0.1 0 0.1 0.2 0.3 0.4 0.5
FOCUS BIAS VOLTAGES (V)

FIG. 10

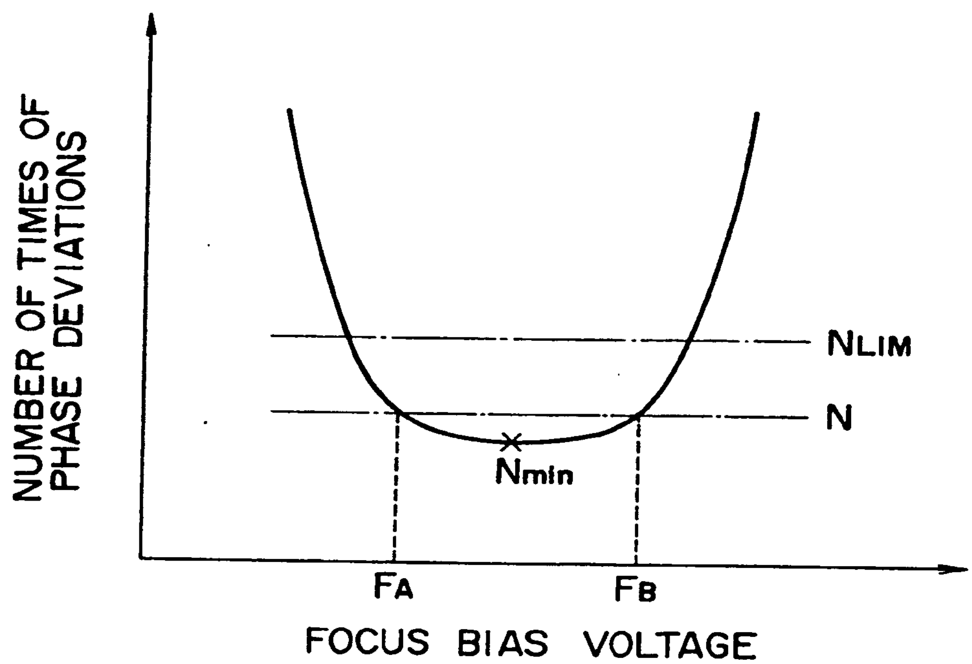
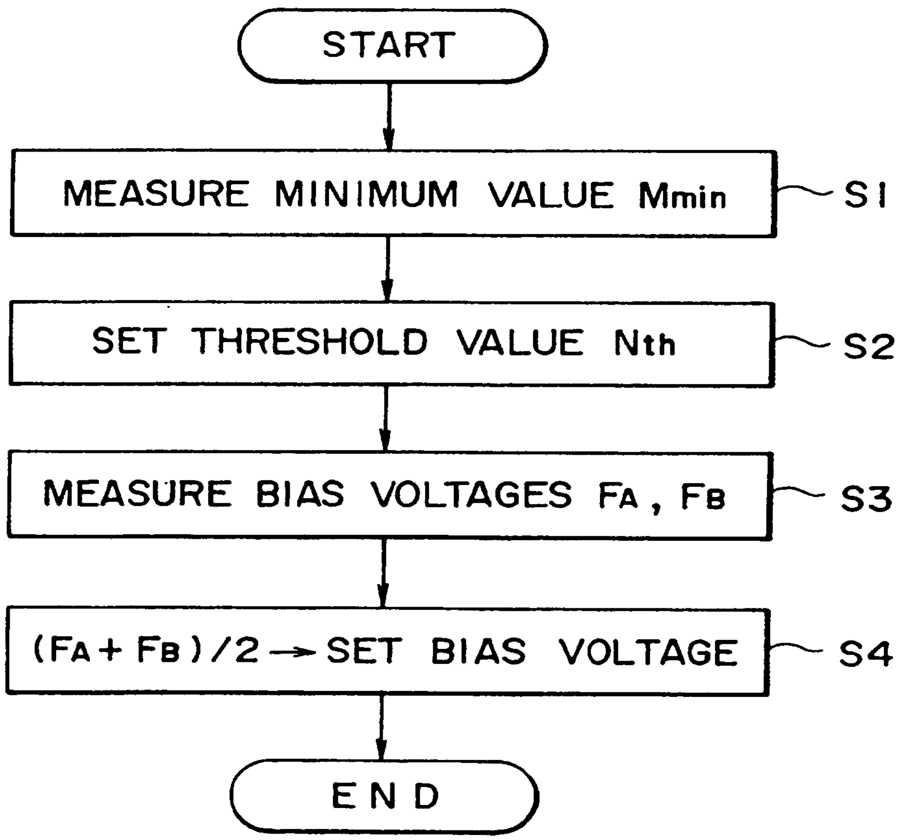

NUMBER OF TIMES OF PHASE DEVIATIONS
NLIM
N
Nmin
FA
FB
FOCUS BIAS VOLTAGE

FIG. 11


START
MEASURE MINIMUM VALUE Mmin
S1
SET THRESHOLD VALUE Nth
S2
MEASURE BIAS VOLTAGES FA, FB
S3
(FA + FB)/2 → SET BIAS VOLTAGE
S4
END

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 10 1651

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	DE-A-41 02 857 (DEUTSCHE THOMSON BRANDT) * the whole document * ---	1	G11B7/09
A	US-A-4 755 980 (T. YOSHIMARU, A. DOI, T. SAITO) * abstract * * column 7, line 14 - column 9, line 35 * * column 10, line 29 - line 63 * ---	1	
A	G. BOUWHUIS 'Principles of Optical Disc Systems' 1986 , ADAM HILGER , BRISTOL * page 58 - page 64 * -----	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)
G11B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 May 1994	Holubov, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)